

FIG. 1
PRIOR ART

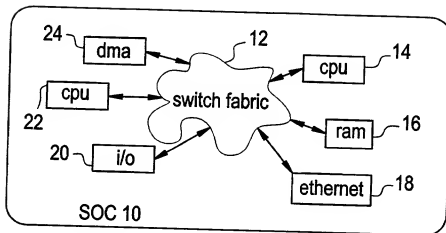
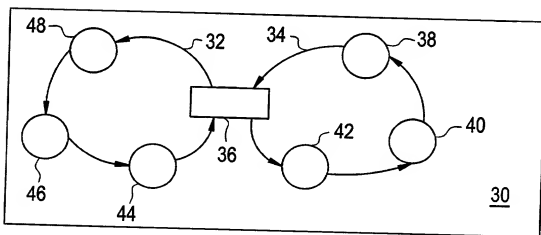


FIG. 2



20126014249001

FIG. 3

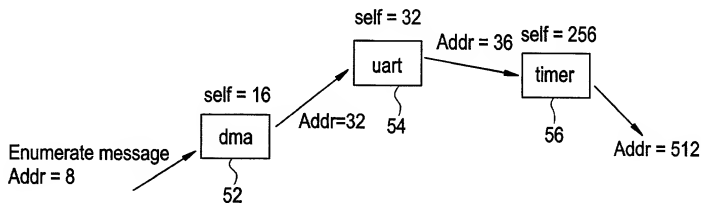


FIG. 4

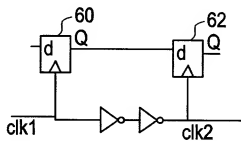
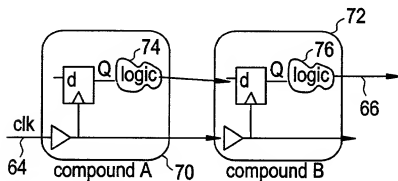


FIG. 5



201260-45349001

FIG. 6

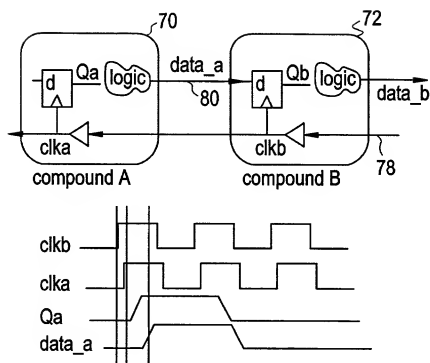


FIG. 7

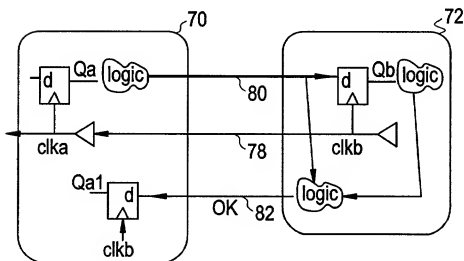


FIG. 8

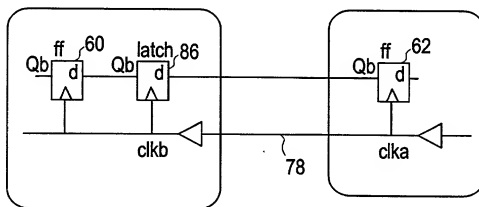


FIG. 9

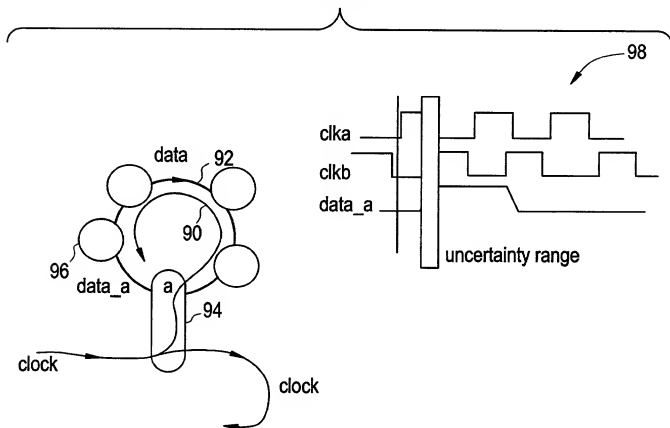


FIG. 10

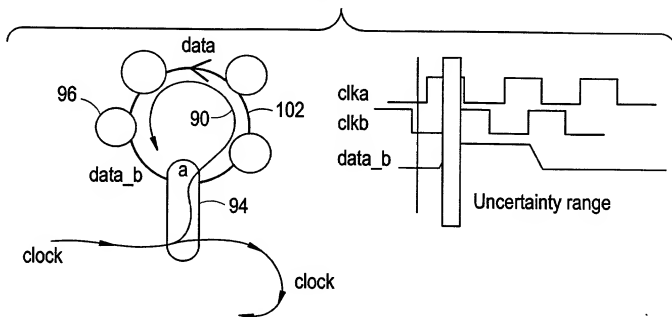


FIG. 11

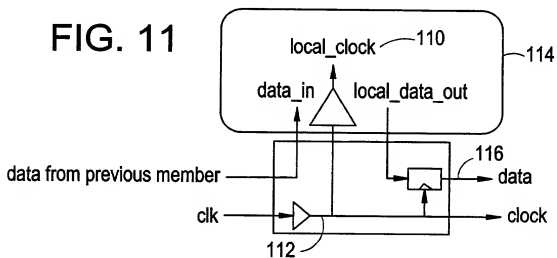


FIG. 12

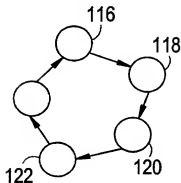


FIG. 13

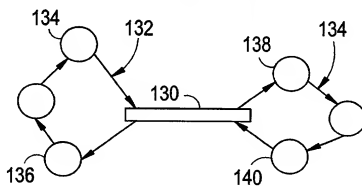


FIG. 14

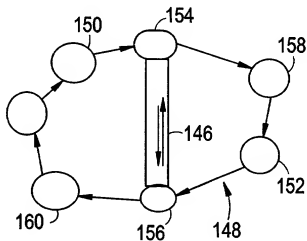


FIG. 15

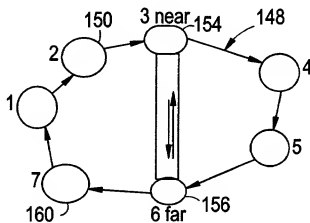


FIG. 16

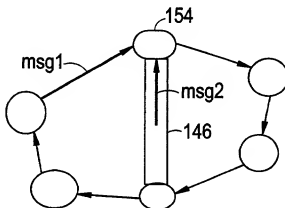


FIG. 17

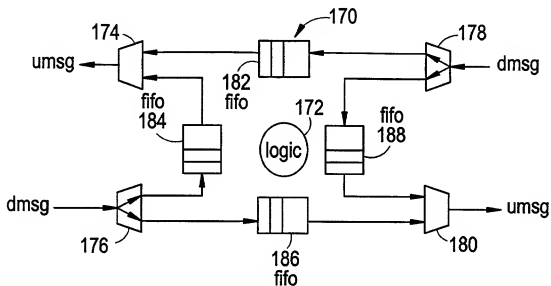


FIG. 18

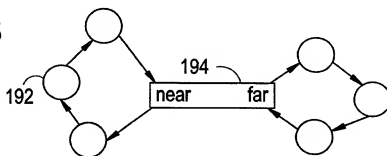


FIG. 19

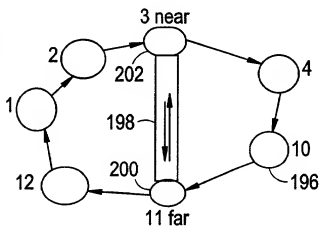


FIG. 20

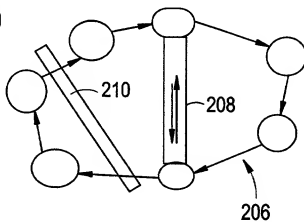


FIG. 21

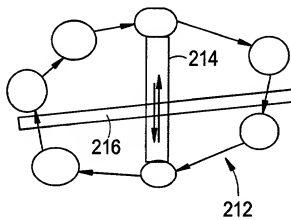
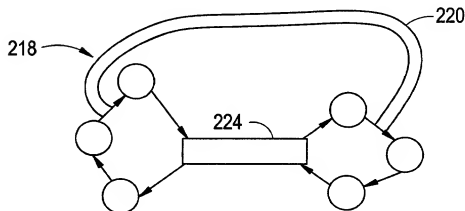


FIG. 22



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FIG. 23

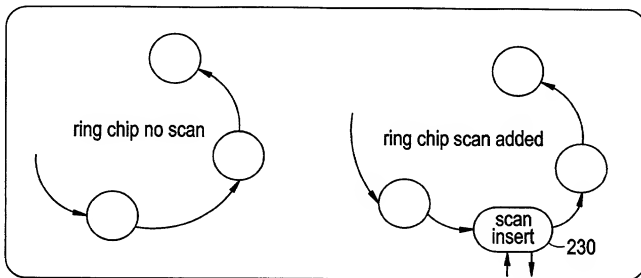


FIG. 24

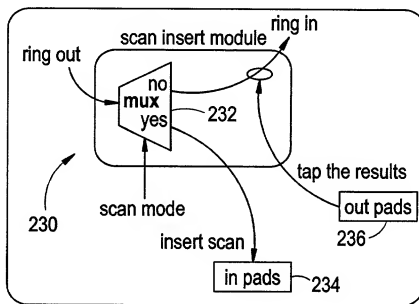
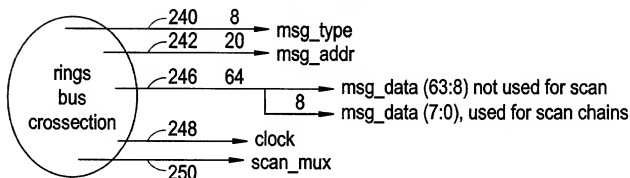


FIG. 25



204260*4E3+9001

FIG. 26

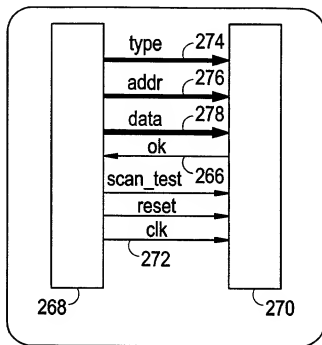
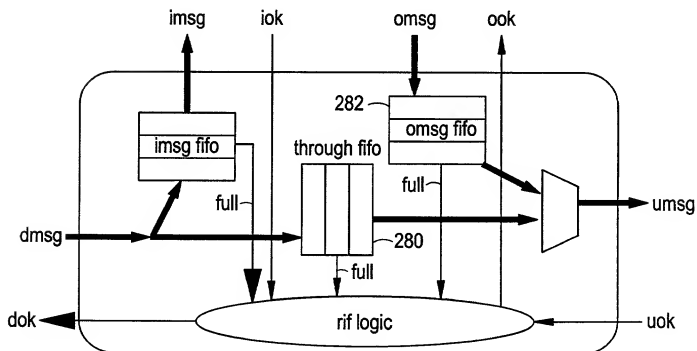


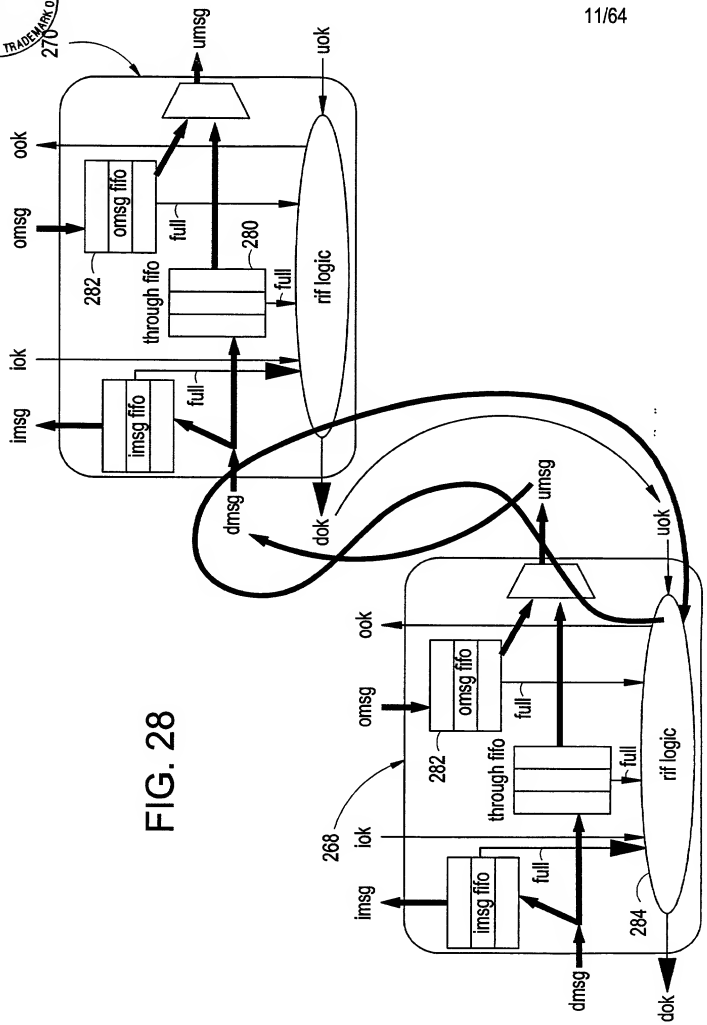
FIG. 27



204260*4E49001

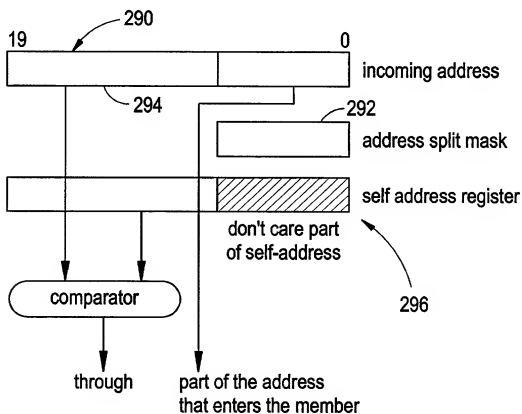


FIG. 28



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FIG. 29



201250-4E-9001

FIG. 30

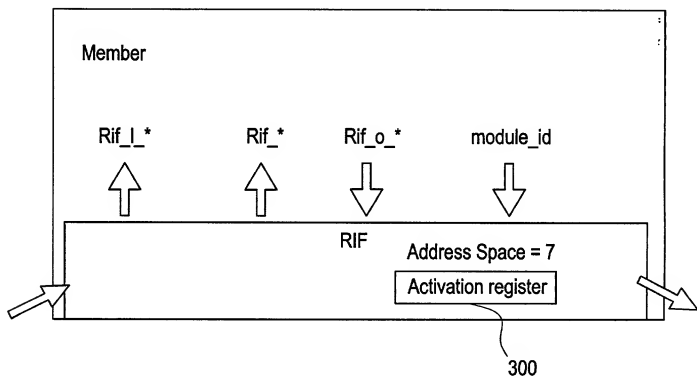


FIG. 31

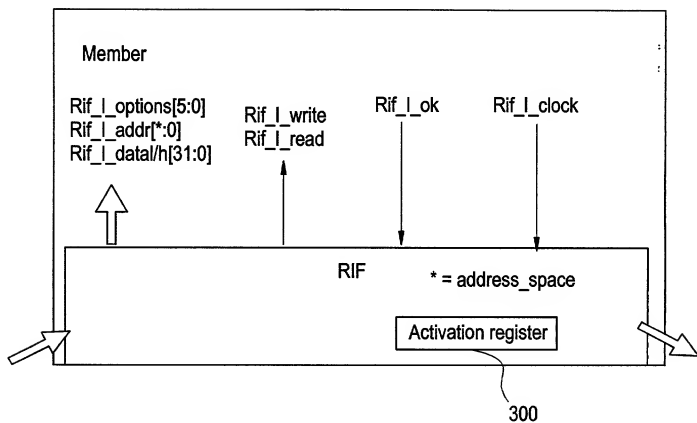


FIG. 32

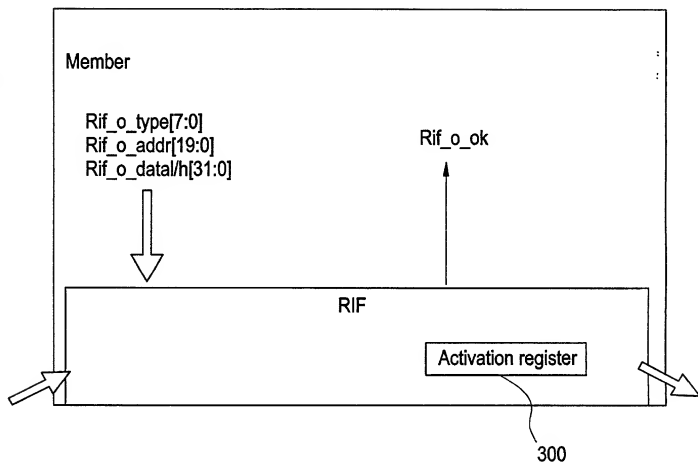
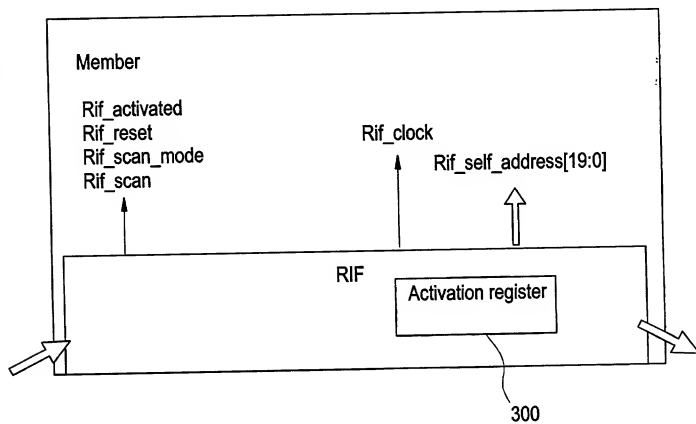


FIG. 33



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FIG. 34

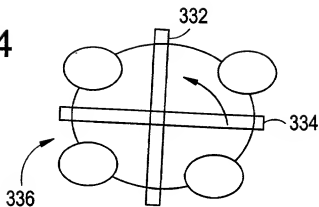


FIG. 35

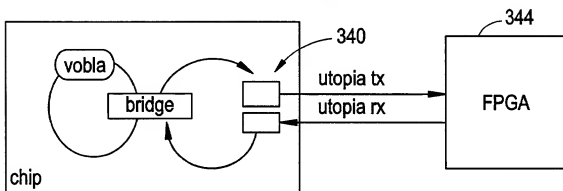
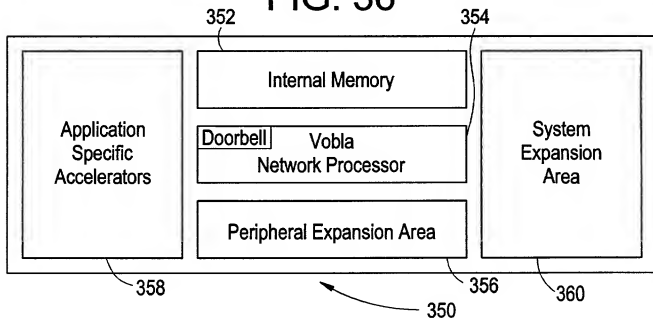
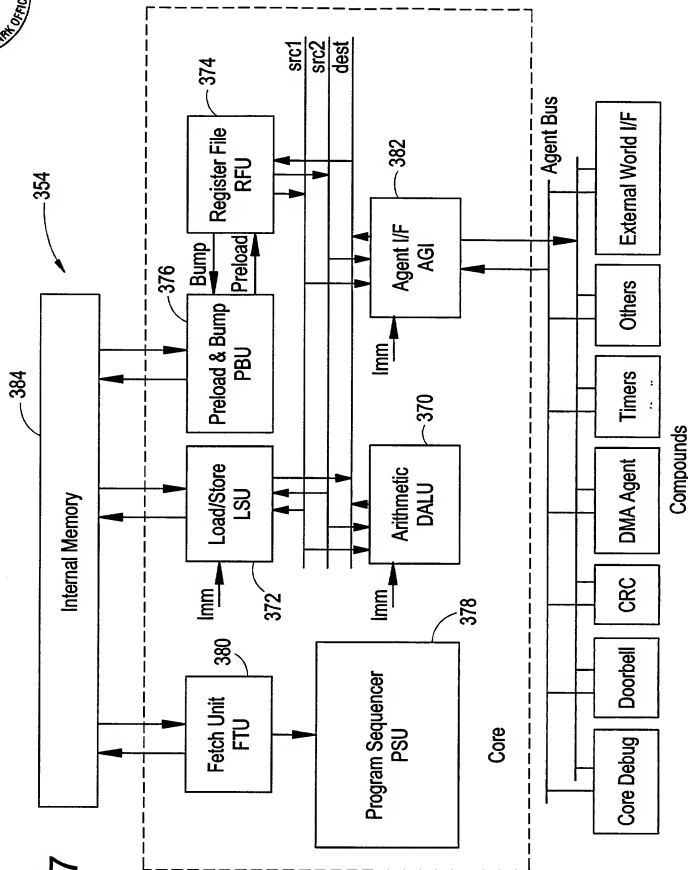


FIG. 36



10064334, 092402

FIG. 37



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2012607429001



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FIG. 38

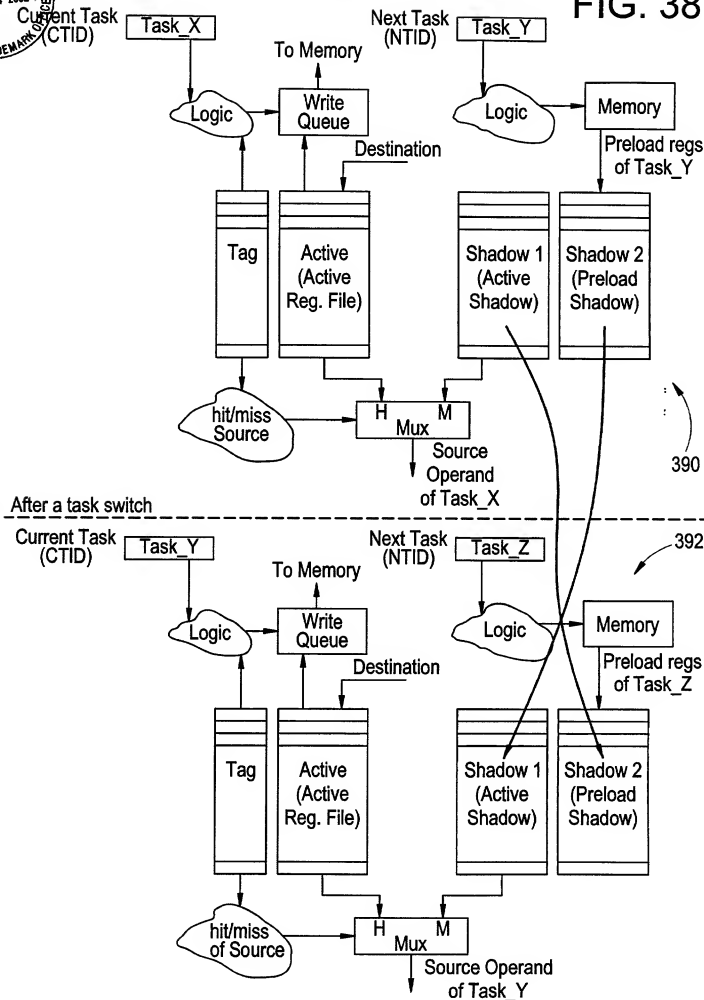


FIG. 39

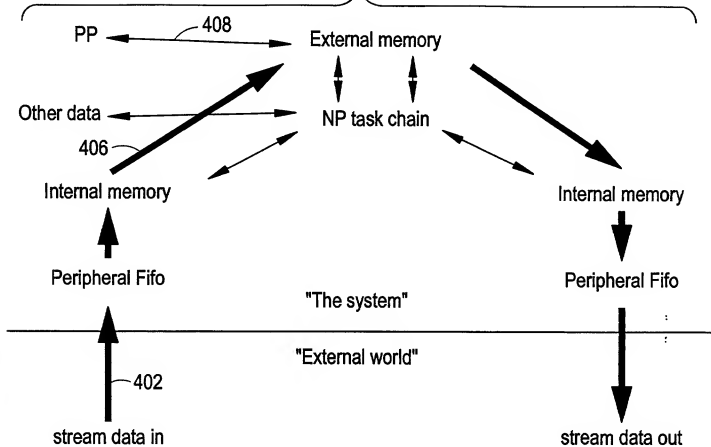
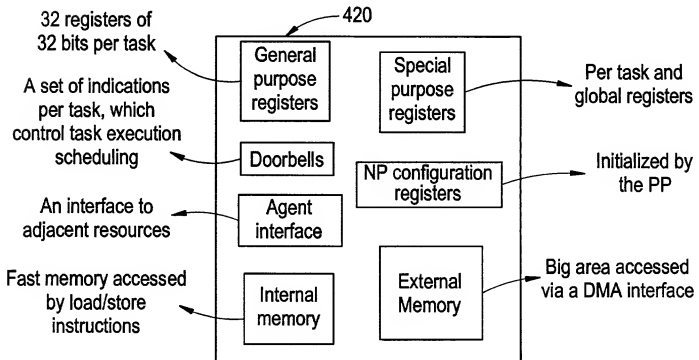


FIG. 40



10061334 02102 20126 4549001

FIG. 41

R1 register

3 3 2 2 2 2 2 2 2 2 2 2 1 1 1 1 1 1 1 1 1 1 9 8 7 6 5 4 3 2 1 0
1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0



s - sticky bit

eq - equal/zero

It - less than/negative

gt - greater than/positive

C - carry

mb - reflection of the RAM mult-reader busy indication

430

FIG. 42

3 3 2 2 2 2 2 2 2 2 2 1 1 1 1 1 1 1 1 1 1 9 8 7 6 5 4 3 2 1 0
1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0

REFETCH SPR
(spr index - 0)

NEXT REFETCH

REFETCH

440

3 3 2 2 2 2 2 2 2 2 2 1 1 1 1 1 1 1 1 1 1 9 8 7 6 5 4 3 2 1 0
1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0

TASK SPR
(spr index - 1)

DOOR BELL REQ	COUNT	UMASK R	NTV	NTID	CTID
---------------------	-------	------------	-----	------	------

442

3 3 2 2 2 2 2 2 2 2 2 1 1 1 1 1 1 1 1 1 9 8 7 6 5 4 3 2 1 0
1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0

TRAP SPR
(spr index - 2)

[illegible]

444

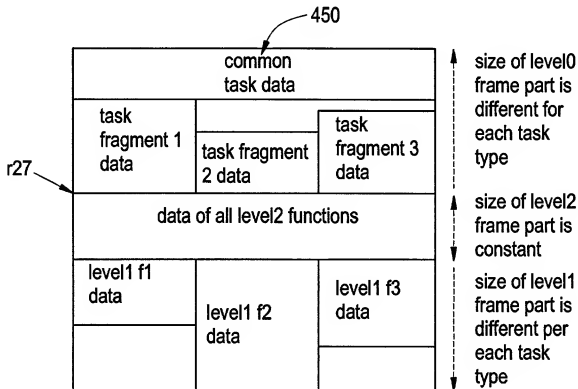
3 3 2 2 2 2 2 2 2 2 2 1 1 1 1 1 1 1 1 1 9 8 7 6 5 4 3 2 1 0
1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0

MINDEX SPR
(spr index - 3)

[illegible]

446

FIG. 43



10061334.052402

FIG. 44

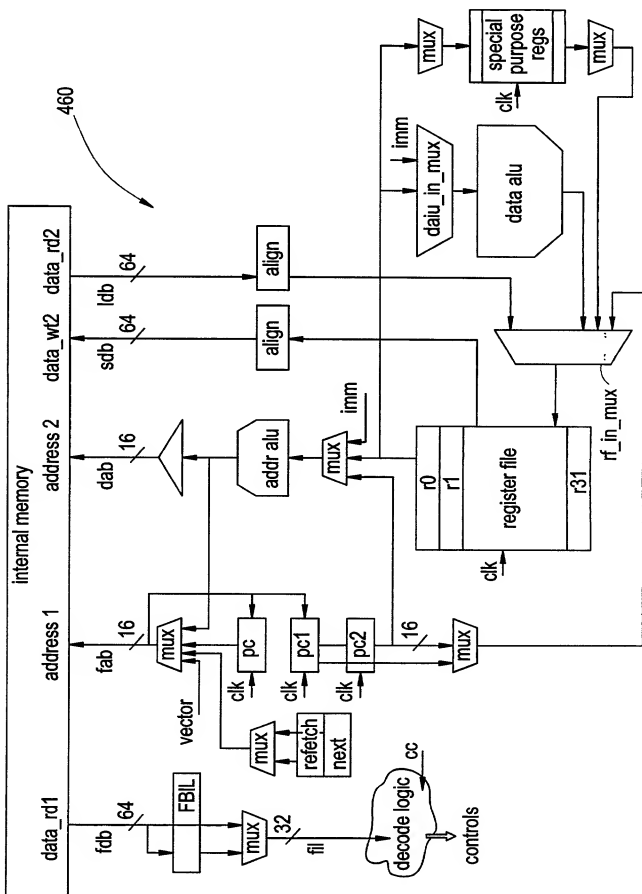


FIG. 45

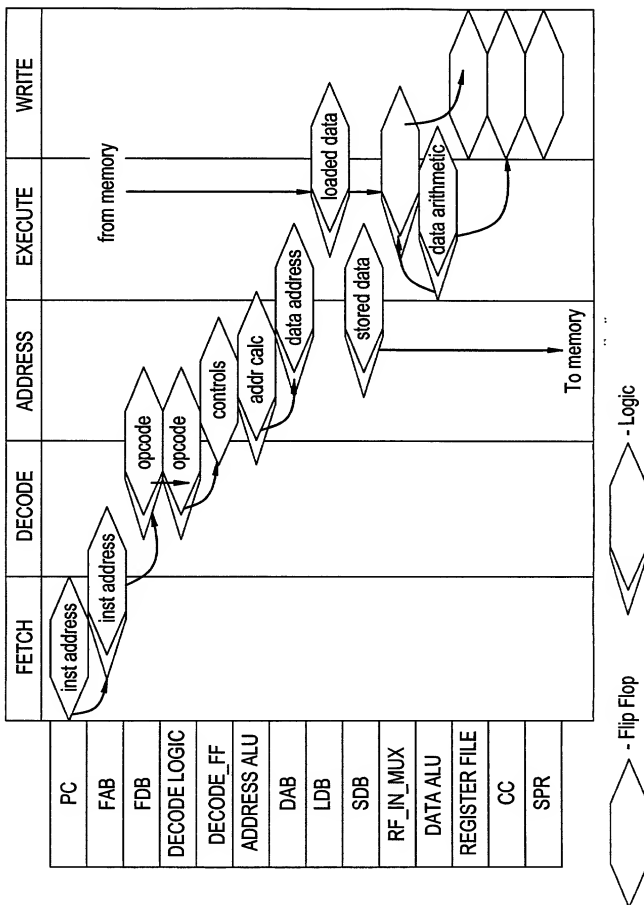


FIG. 46

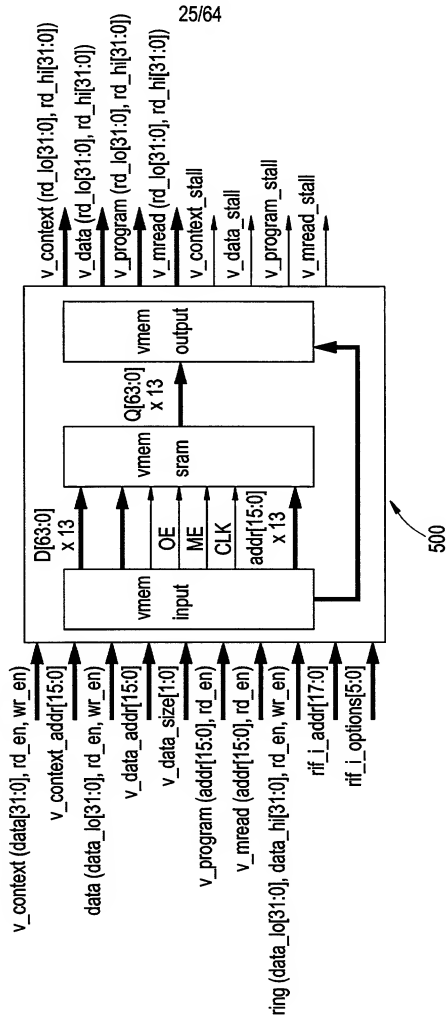


FIG. 47

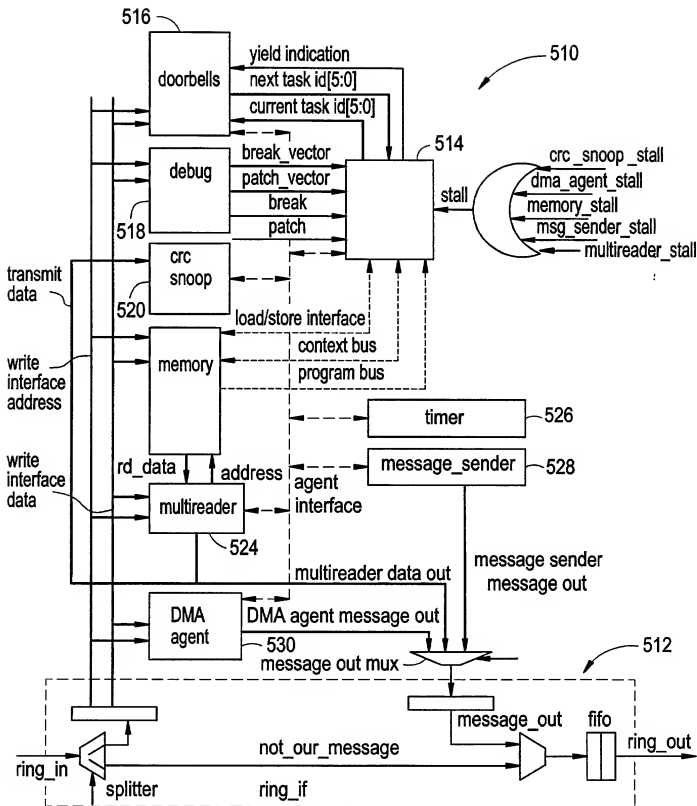


FIG. 48

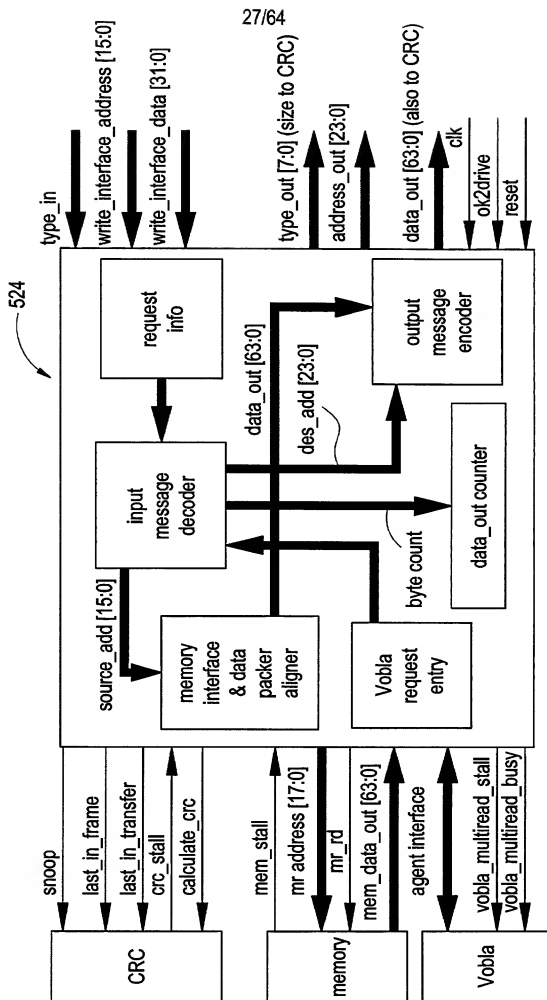


FIG. 49

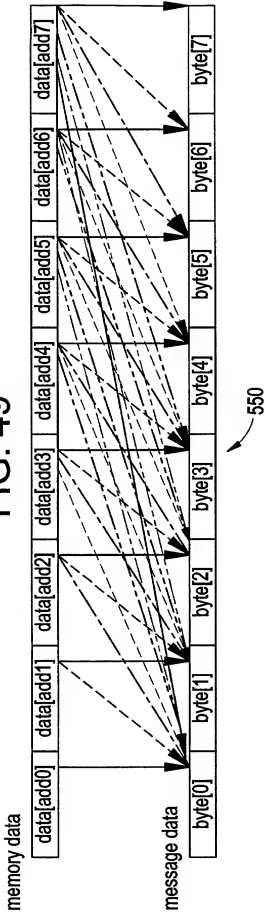


FIG. 50

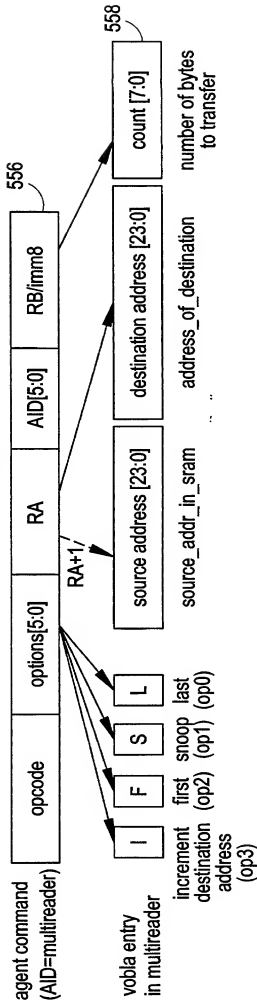


FIG. 51

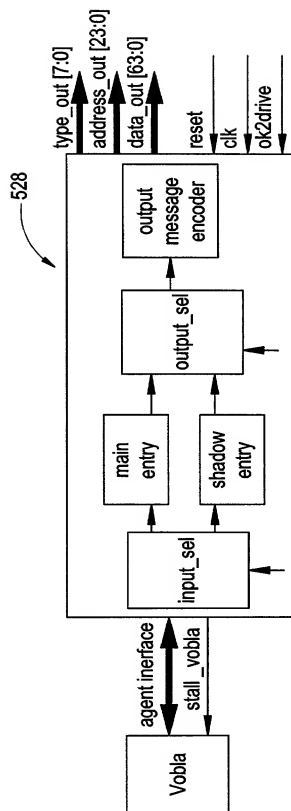


FIG. 52

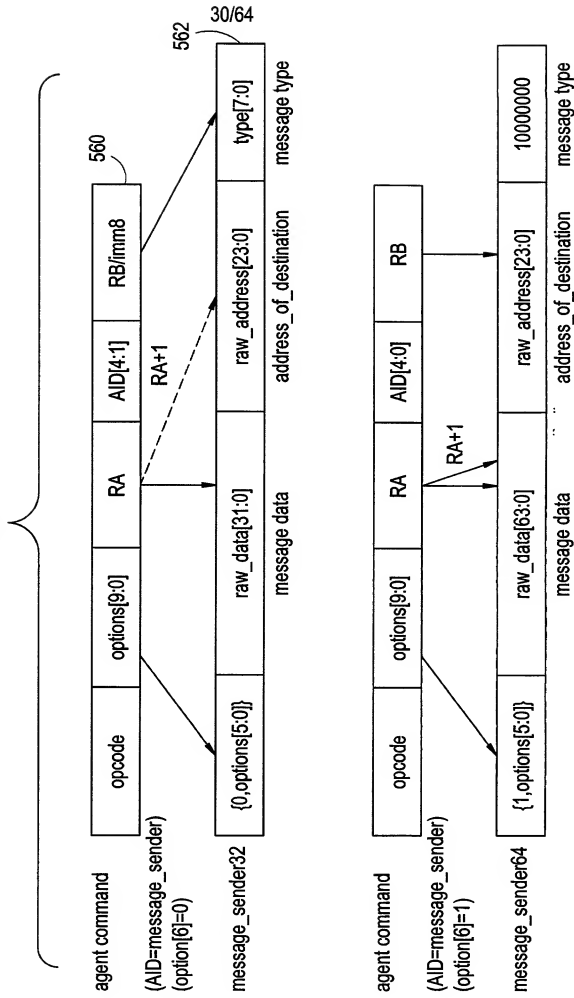


FIG. 53

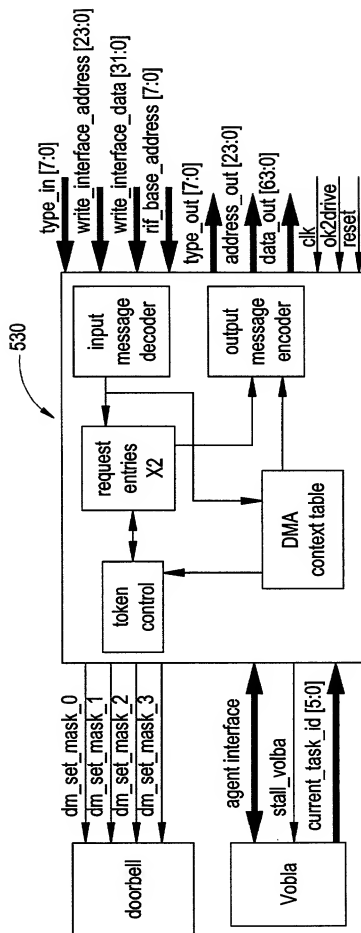


FIG. 54

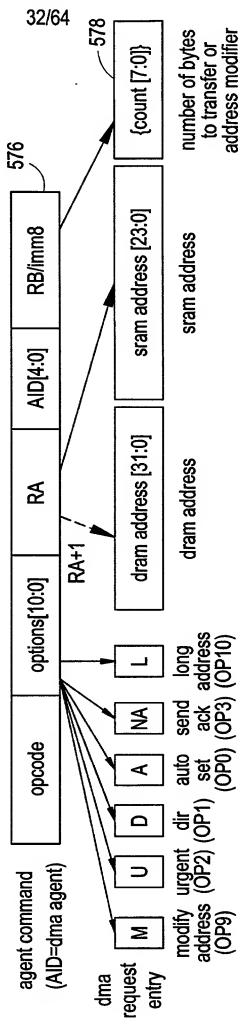


FIG. 55

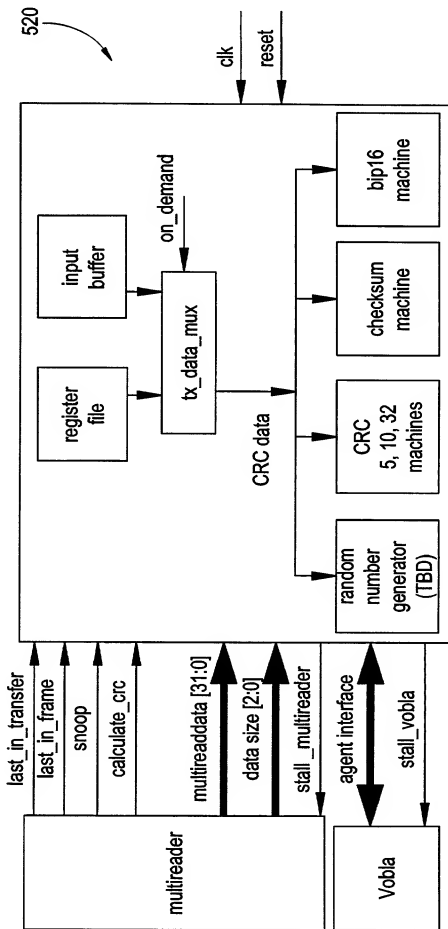


FIG. 57

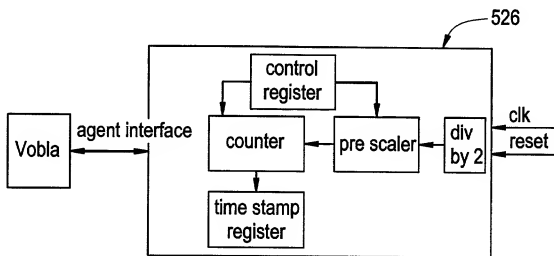


FIG. 58

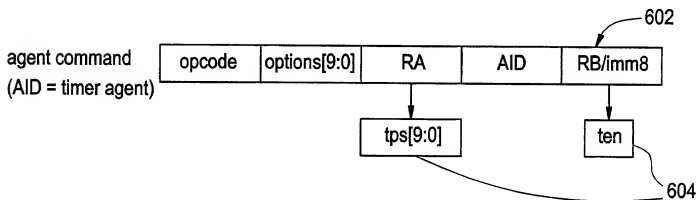


FIG. 59

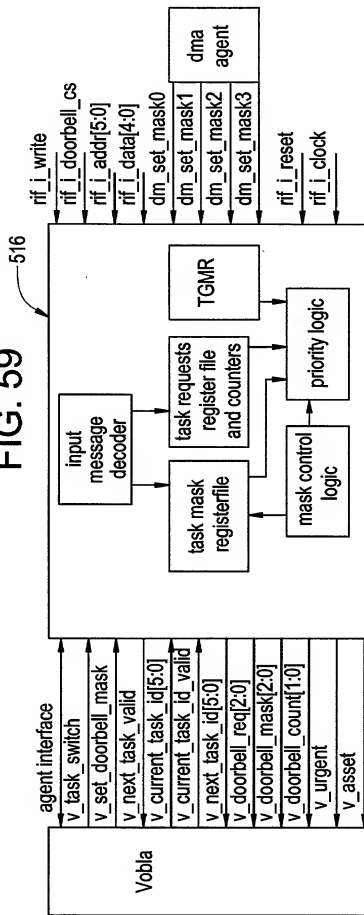


FIG. 60

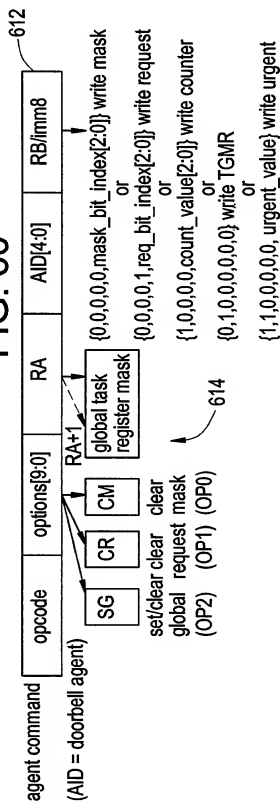
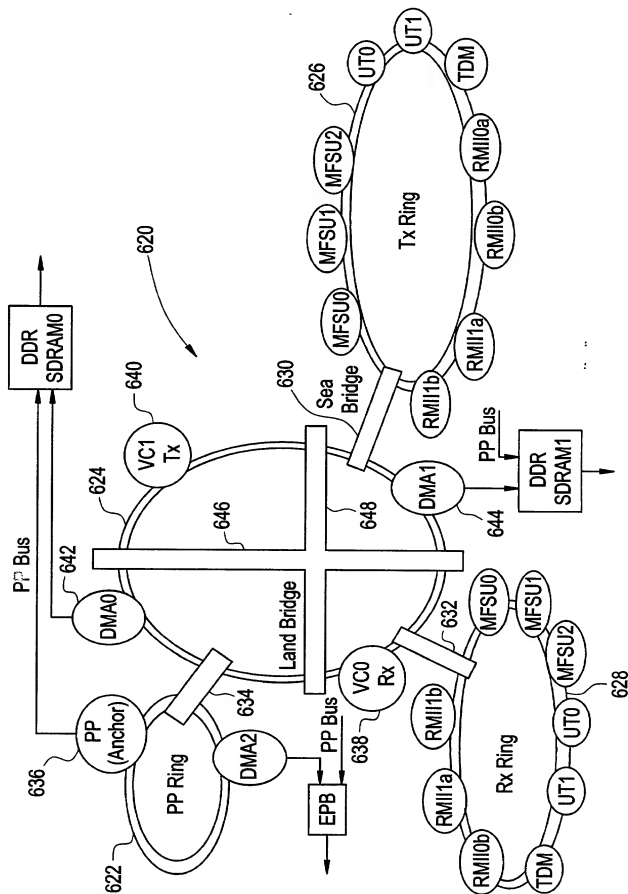


FIG. 61



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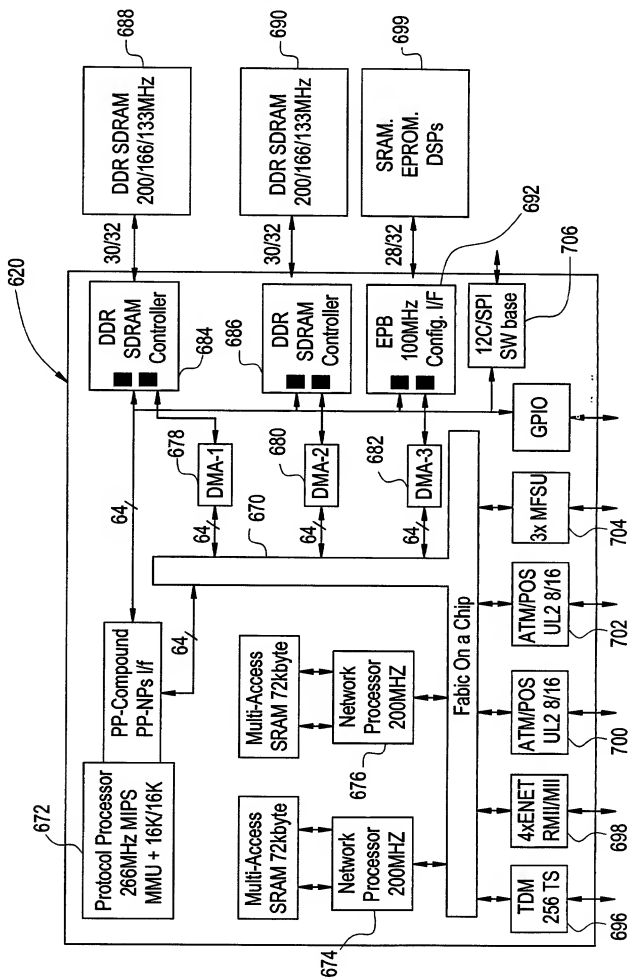


FIG. 63

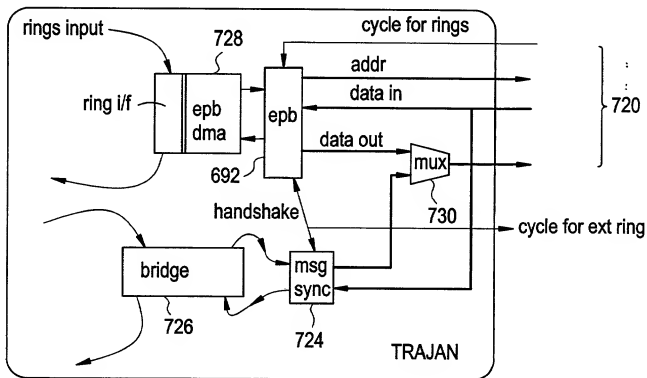
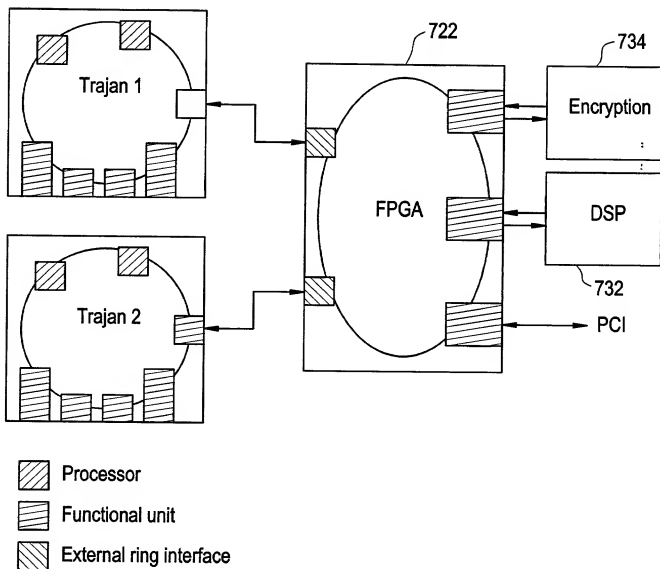


FIG. 64



10064234-092402

FIG. 65

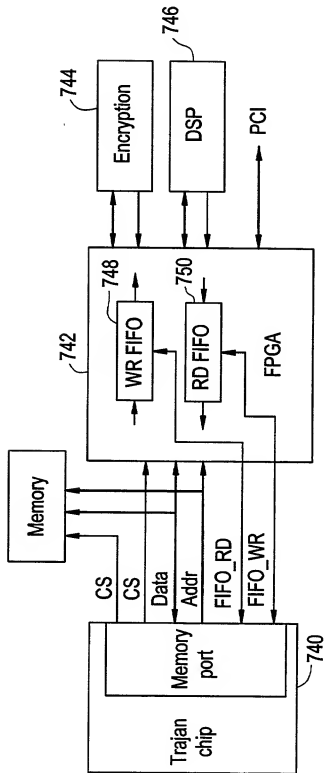


FIG. 66

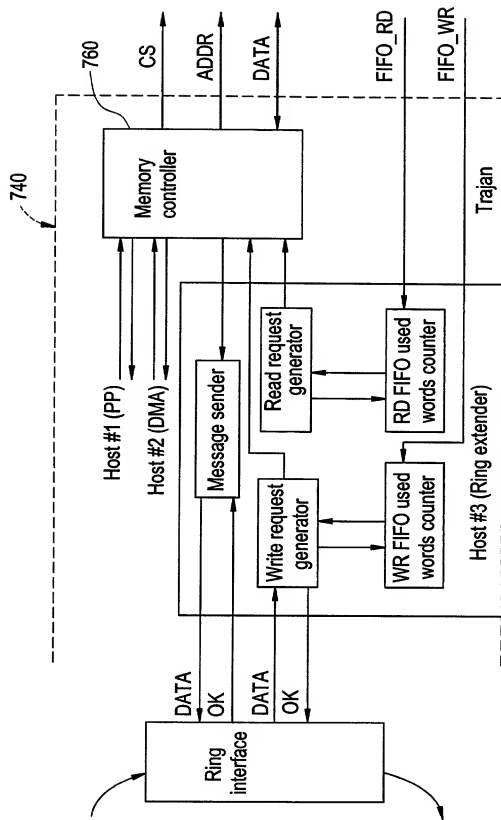


FIG. 67

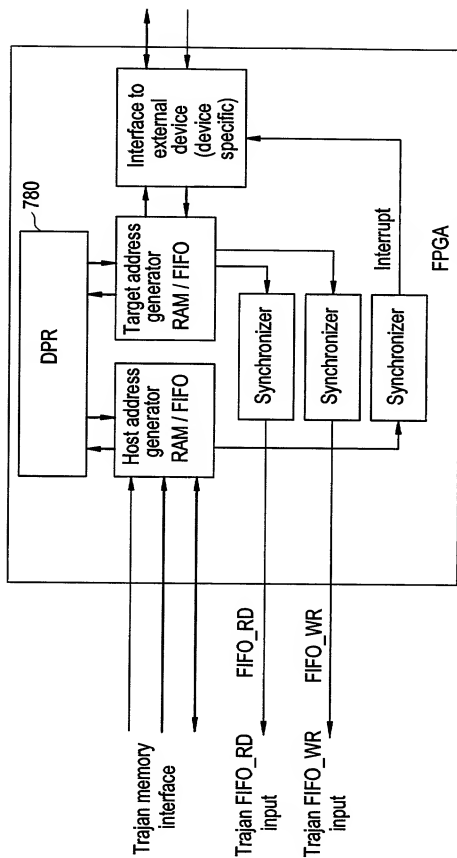


FIG. 68

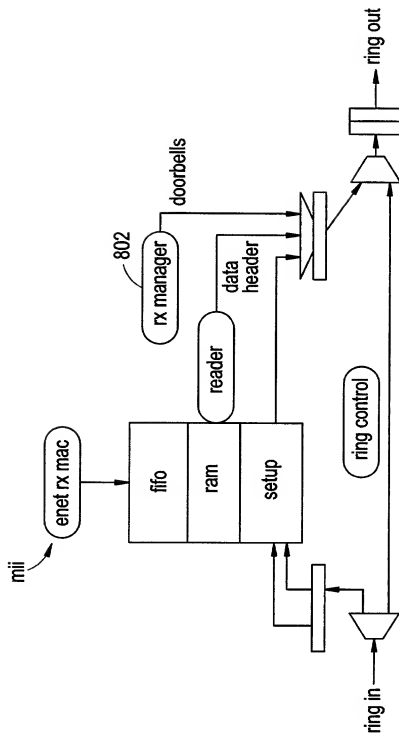


FIG. 69

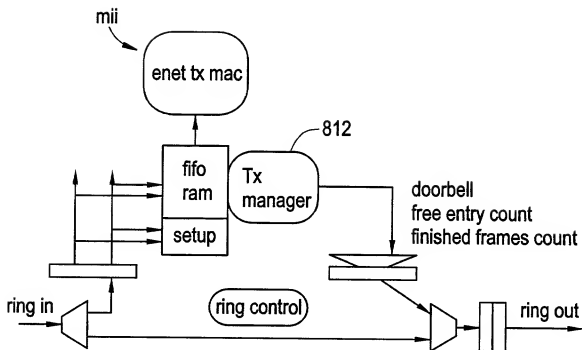
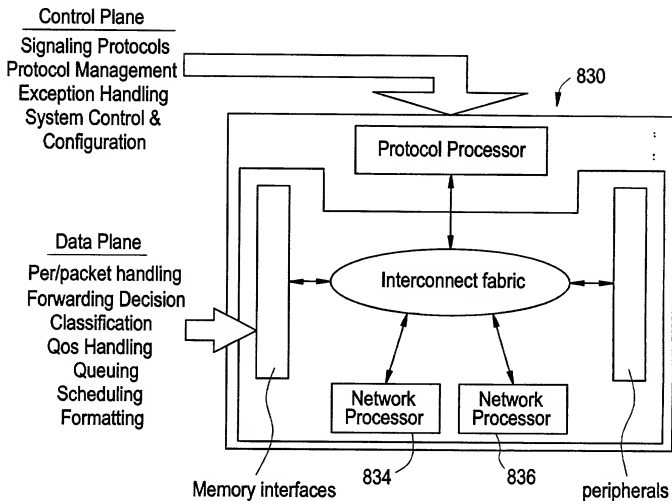


FIG. 70



10064334.002402

FIG. 71

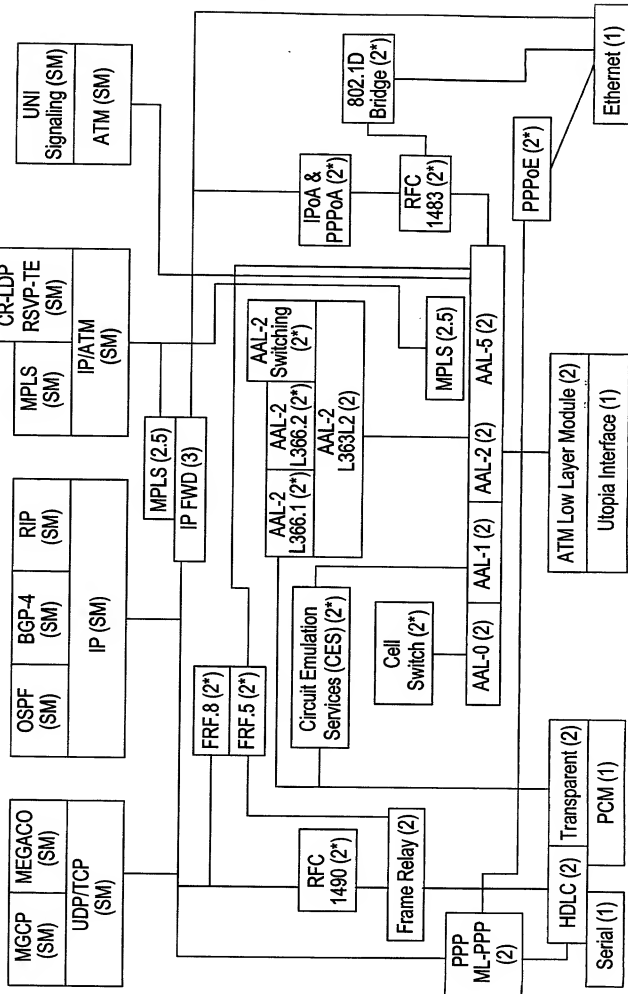


FIG. 72

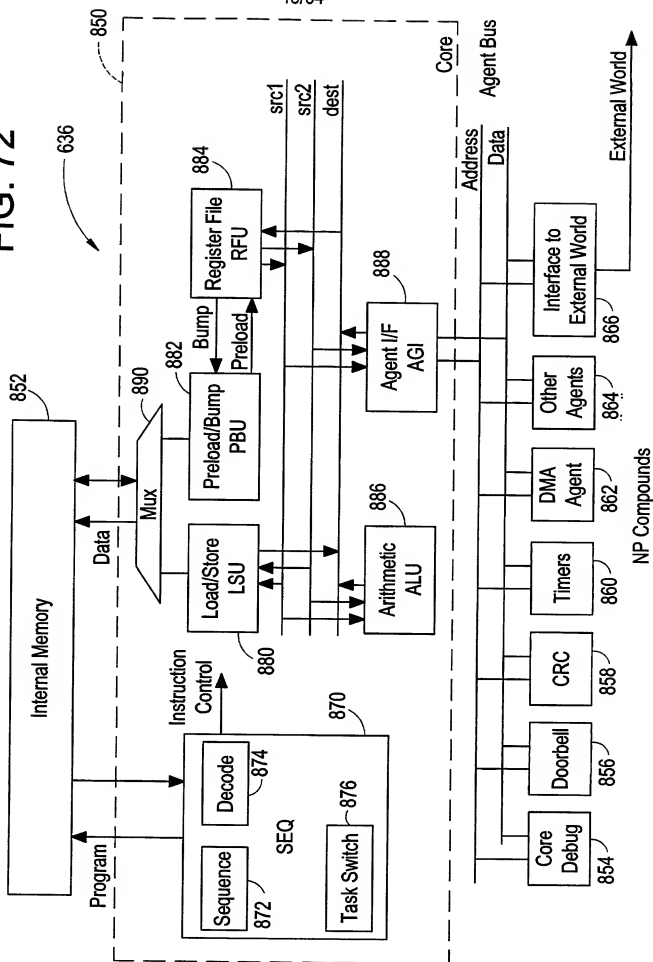


FIG. 73

900

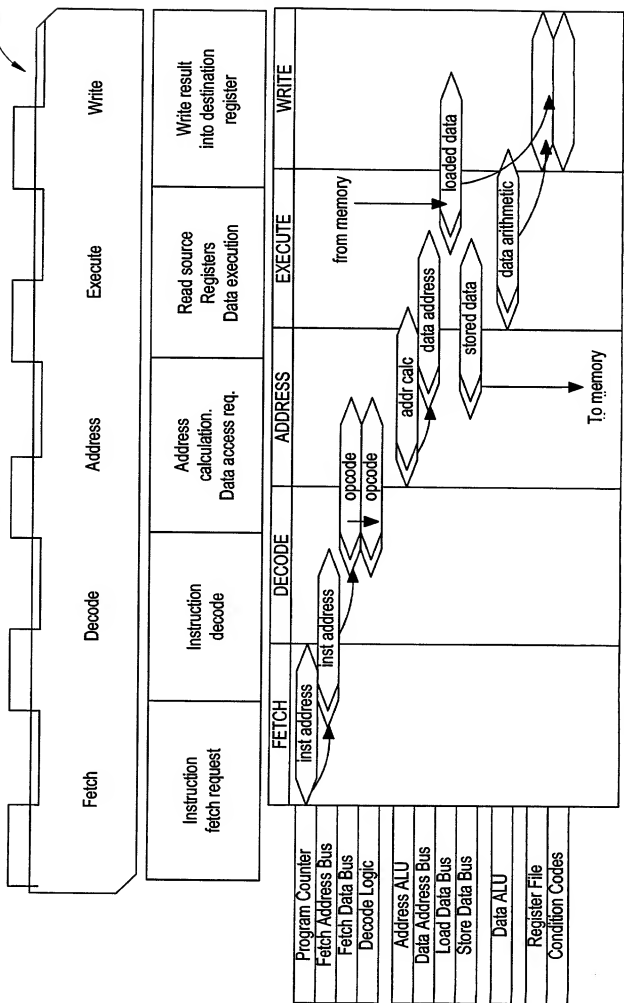


FIG. 74

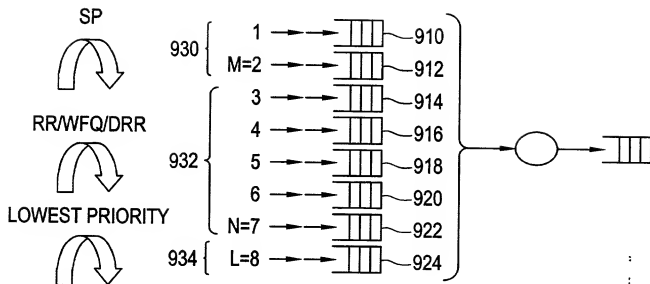


FIG. 75

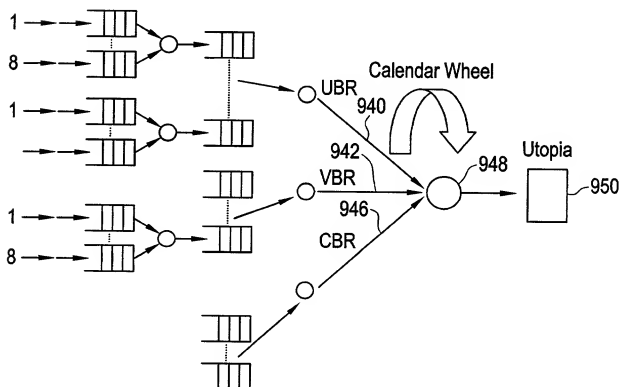


FIG. 76

960

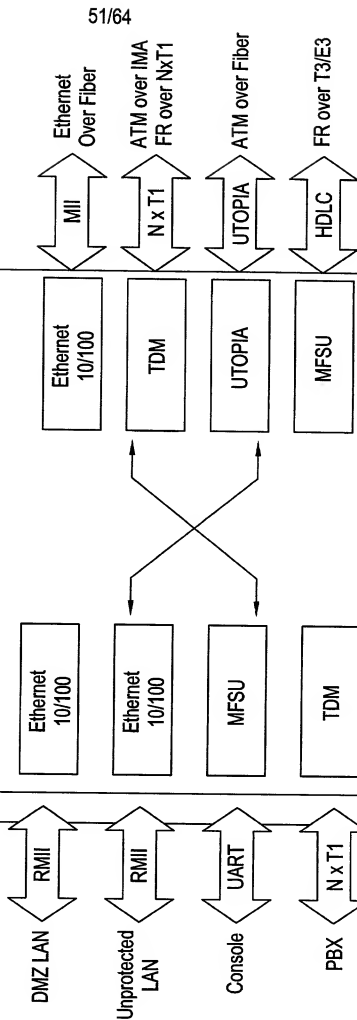


FIG. 77

970

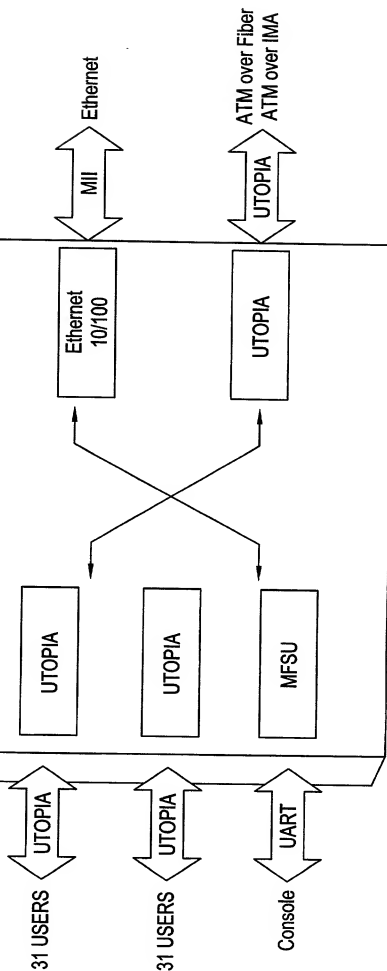
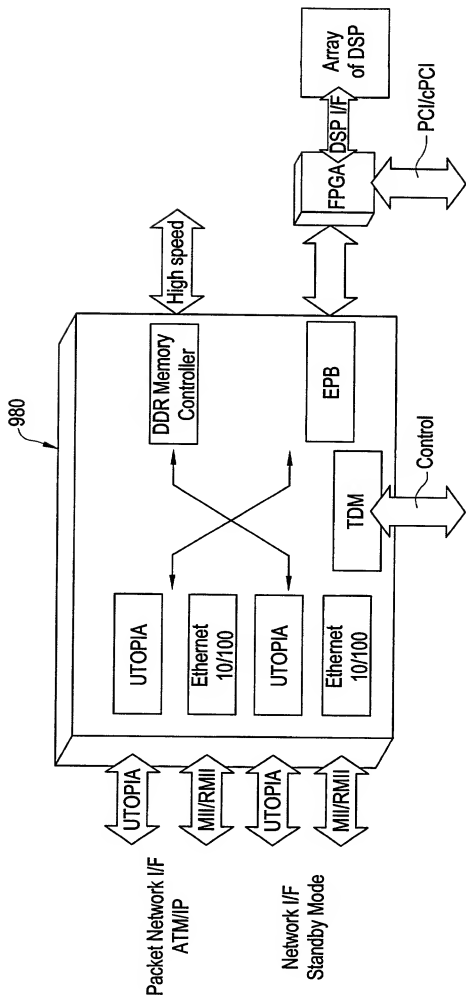


FIG. 78



204250 "net9001"

FIG. 79

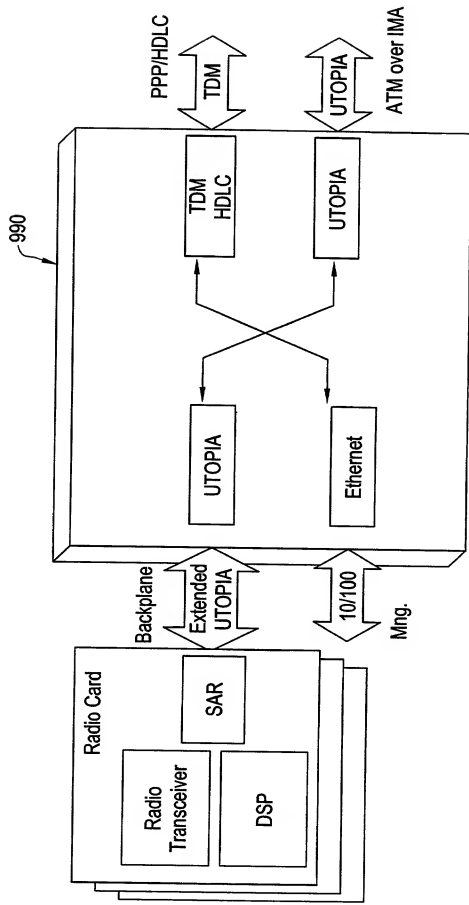


FIG. 80

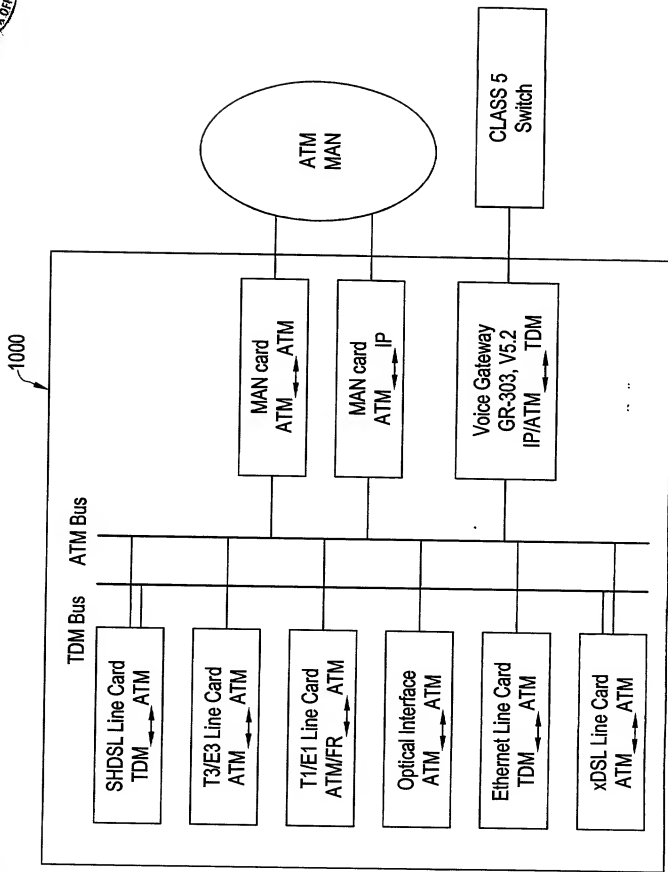


FIG. 81

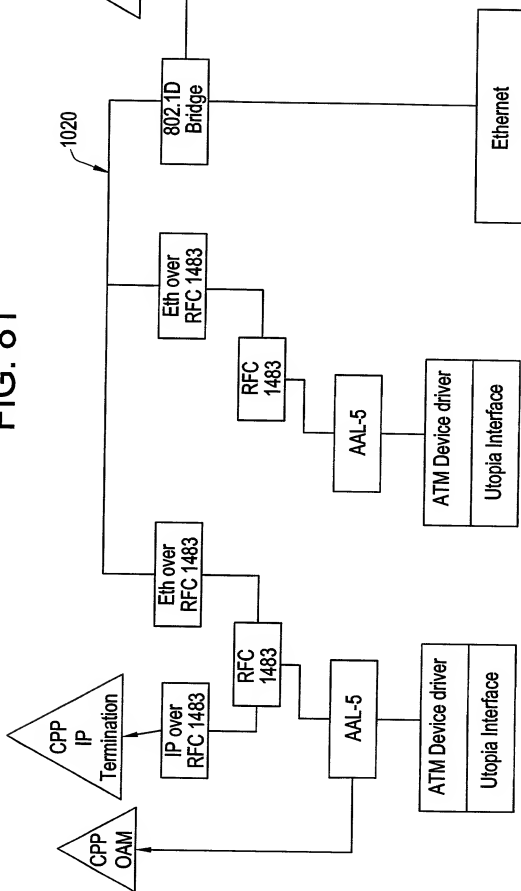
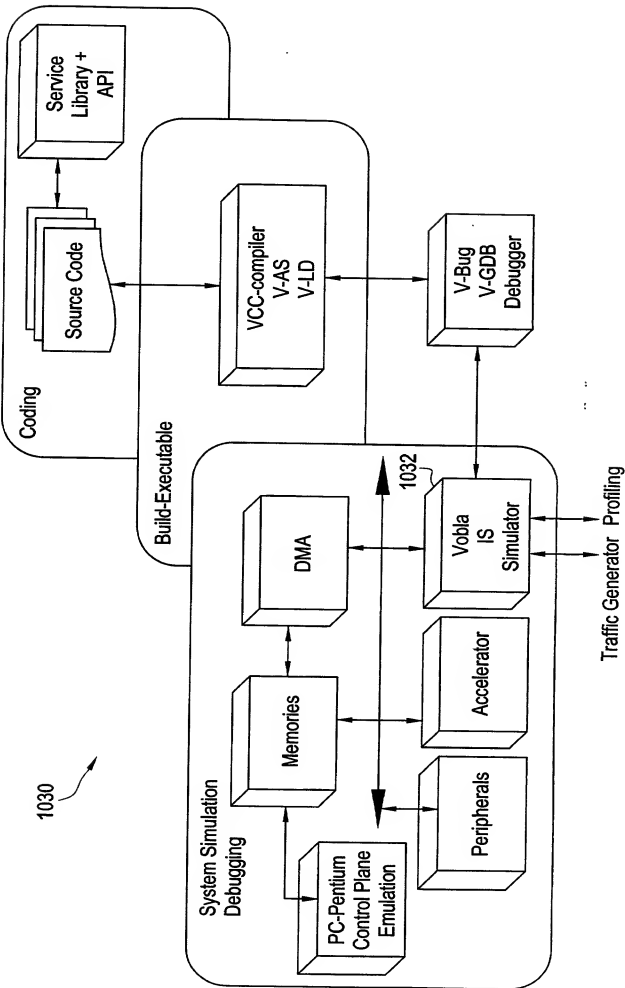


FIG. 82



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FIG. 83

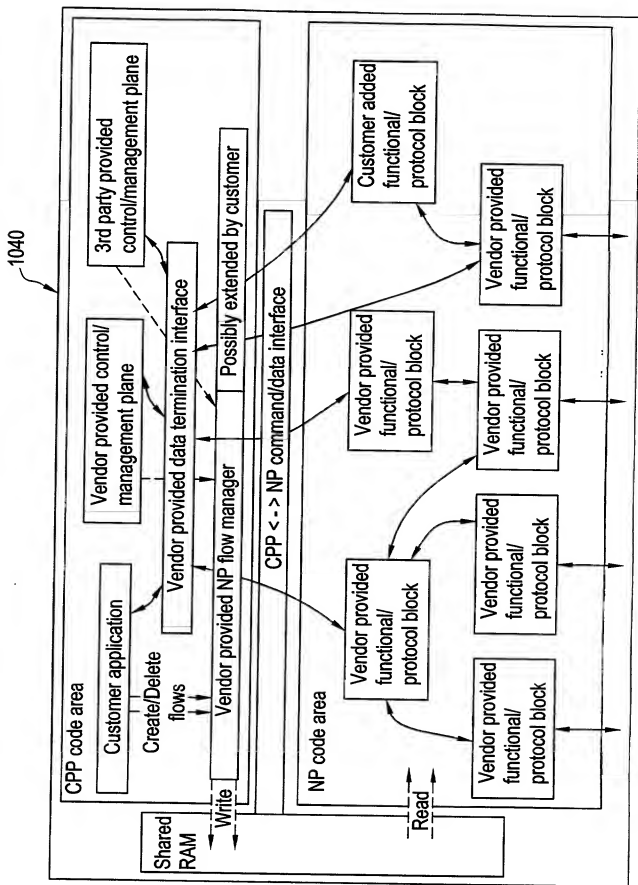
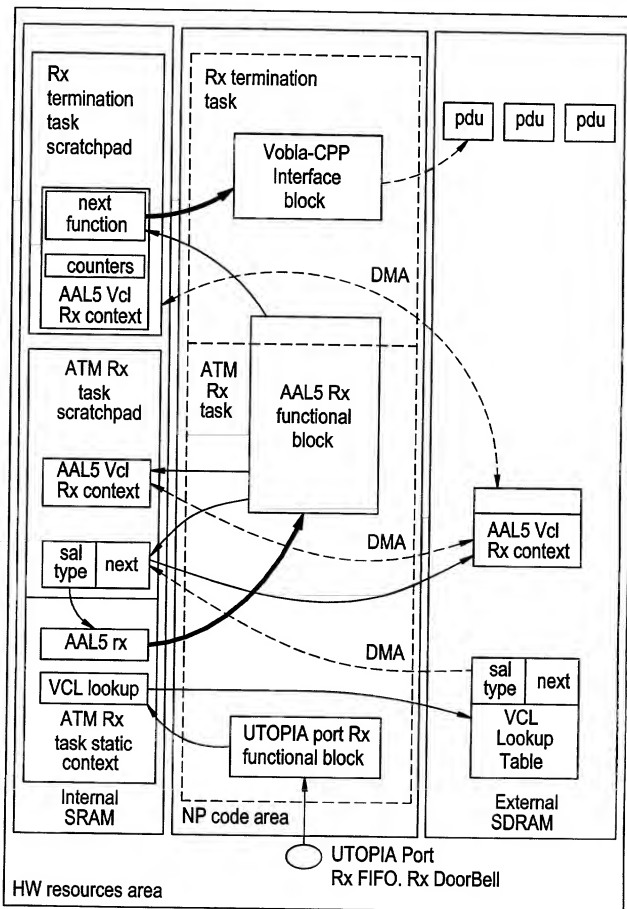


FIG. 84

1050



10064331-092102

FIG. 85

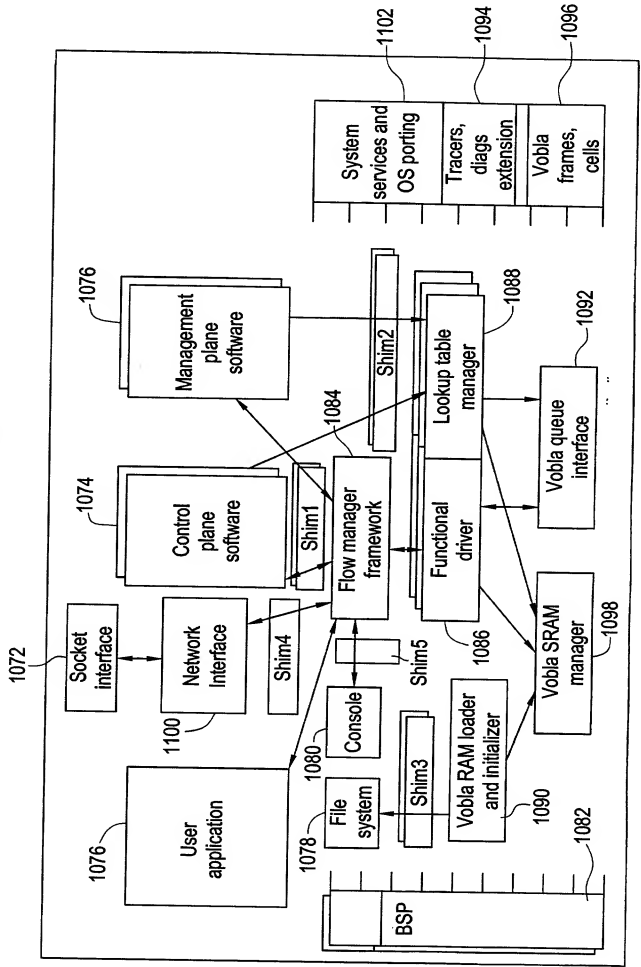


FIG. 86

1200

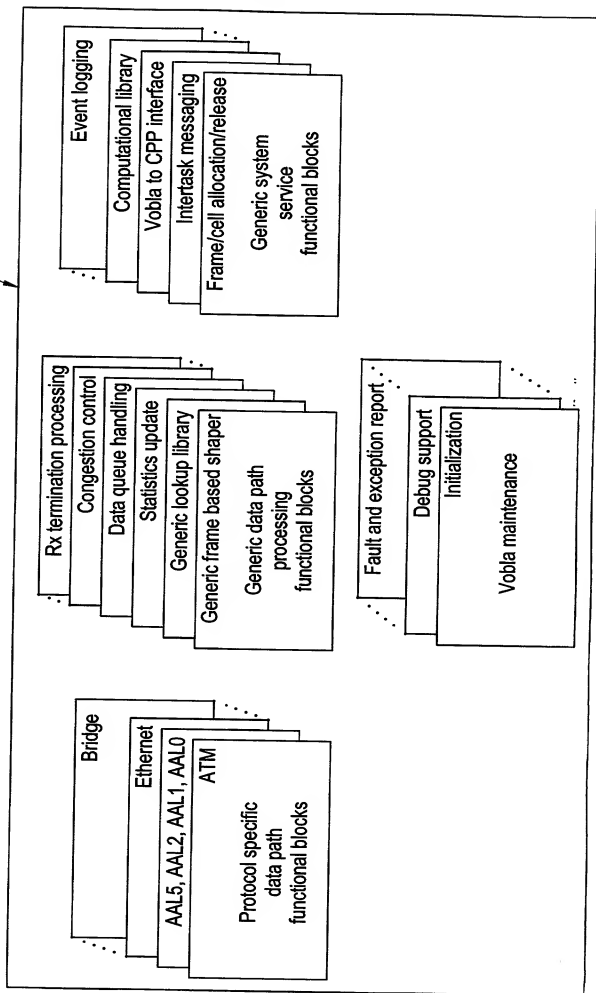


FIG. 87

PRIOR ART

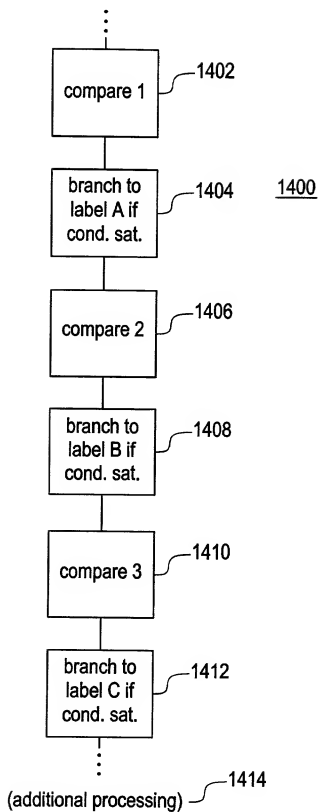


FIG. 88

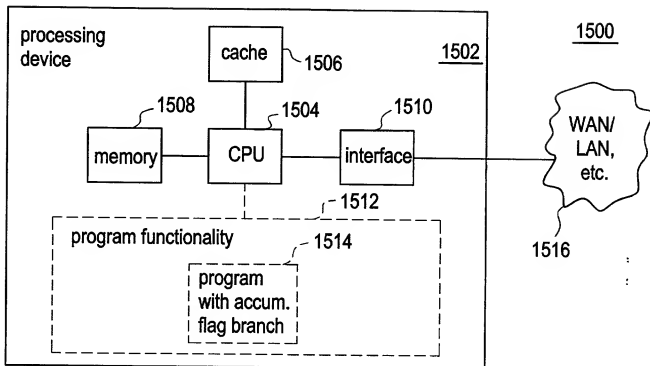


FIG. 89

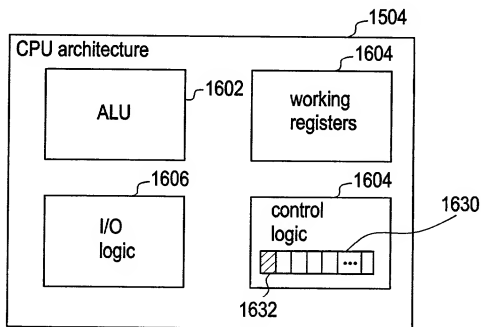


FIG. 90

